CLAIMS

[0058] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An integrated circuit comprising:

a substrate comprising a lower layer and an upper layer on the lower layer;

an array of pixel cells at a surface of the upper layer, each pixel cell comprising a photo-conversion device; and

a trench structure around at least a portion of the array, wherein the trench structure extends from the surface to the lower layer, and wherein the trench structure prevents at least a portion of photons or charged particles from passing through the trench structure to the array.

2. The integrated circuit of claim 1, wherein the trench structure has sidewalls and contains a first material that prevents at least a portion of photons or charged particles from passing through the trench structure to the array.

3. The integrated circuit of claim 2, further comprising a liner formed along at least a portion of the sidewalls.
4. The integrated circuit of claim 3, wherein the liner is a high absorption material.
5. The integrated circuit of claim 2, further comprising a thermal oxide on the sidewalls of the trench structure.
6. The integrated circuit of claim 2, wherein the first material is selected from the group consisting of doped polysilicon, undoped polysilicon and boron-doped carbon.
7. The integrated circuit of claim 2, further comprising a second material that partially fills the trench structure, wherein the second material prevents at least a portion of photons or charged particles from passing through the trench structure to the array.
8. The integrated circuit of claim 7, wherein the second material has a higher refractive index than that of the first material.
9. The integrated circuit of claim 7, further comprising a third material that partially fills the trench structure,

wherein the third material prevents at least a portion of photons or charged particles from passing through the trench structure to the array.

10. The integrated circuit of claim 9, wherein the third material has a higher refractive index than that of the second material.

11. The integrated circuit of claim 1, wherein the trench structure has a depth of about 4μm to about 6μm.

12. The integrated circuit of claim 1, wherein the integrated circuit comprises one of a CMOS image sensor and a CCD image sensor.

13. A structure for isolating an active area of an integrated circuit, the structure comprising:

a trench formed in a substrate of the integrated circuit along at least a portion of a periphery of the active area, the substrate having a lower layer and an upper layer on the lower layer, wherein the trench extends from a surface of the upper layer to a surface of the lower layer;

an insulating liner formed along sidewalls of the trench; and

a first fill material formed over the insulating liner wherein the first fill material at least partially fills the trench and prevents at least a portion of photons and electrons from passing through the trench to the active area.

14. The structure of claim 13, wherein the insulating liner is a high absorption material.

15. The structure of claim 13, further comprising a thermal oxide material on the sidewalls of the trench.

16. The structure of claim 13, wherein the first fill material is an attenuating material that absorbs photons.

17. The structure of claim 16, wherein the first fill material comprises one of doped polysilicon, undoped polysilicon and boron-doped carbon.

18. The structure of claim 13, wherein the trench has a depth of about 4μm to about 6μm.

19. The structure of claim 13, further comprising a second fill material that partially fills the trench, wherein the second

material prevents at least a portion of photons from passing through the trench.

20. The structure of claim 19, wherein the second fill material has a higher refractive index than that of the first material and is deposited over the surface of the first fill material.

21. The structure of claim 19, further comprising a third fill material that partially fills the trench, wherein the third fill material prevents at least a portion of photons from passing through the trench.

22. The structure of claim 21, wherein the third fill material has a higher refractive index than that of the second material and is deposited over the surface of the second fill material.

23. The structure of claim 13, wherein the semiconductor device comprises one of a CMOS image sensor, a CCD image sensor, a DRAM, a flash memory, an SRAM, a microprocessor, a DSP and an ASIC.

24. A structure for isolating an active area on an integrated circuit, the structure comprising:

a plurality of trenches formed in a substrate of the integrated circuit on at least a portion of a periphery of the active area, wherein each of the plurality of trenches extends to a surface of a base layer below the substrate.

25. The structure according to claim 24, further comprising an insulating liner formed along each sidewall of the plurality of trenches.

26. The structure according to claim 25, wherein the insulating liner comprises a high absorption material.

27. The structure according to claim 25, wherein the insulating liner comprises a light attenuation film.

28. The structure according to claim 25, wherein the insulating liner comprises a nitride material or alpha carbon material.

29. The structure according to claim 24, further comprising a first fill material that at least partially fills each of the plurality of trenches and prevents at least a portion of

photons or charged particles from passing through the trench.

30. The structure according to claim 29, wherein the first fill material is a high absorption material.

31. The structure according to claim 29, wherein the first fill material is a high extinction coefficient material.

32. The structure according to claim 29, wherein the first fill material is one of doped polysilicon, undoped polysilicon and boron-doped carbon.

33. The structure according to claim 29, further comprising a second fill material that partially fills each of the plurality of trenches, wherein the second material prevents at least a portion of photons from passing through the trench.

34. The structure according to claim 33, wherein the second fill material has a higher refractive index than that of the first material.

35. The structure according to claim 33, further comprising a third fill material that partially fills each of the plurality of trenches, wherein the third fill material prevents at

least a portion of photons from passing through the trench.

36. The structure according to claim 35, wherein the third fill material has a higher refractive index than that of the second material.

37. The structure according to claim 24, wherein each of the trenches has a depth of about 4μm to about 6μm.

38. A processing system, the processing system comprising:

a processor;

an integrated circuit coupled to the processor, the integrated circuit comprising a structure for isolating an active area on the integrated circuit, the structure comprising:

a trench formed in a substrate on at least a portion of a periphery of the active area of the integrated circuit, wherein the trench extends to a surface of a base layer below the substrate, and wherein the trench has sidewalls;

an insulating liner formed along the sidewalls; and

a first fill material formed over the insulating liner that at least partially fills the trench and prevents at least a portion of photons or electrons from passing through the trench.

39. The processing system of claim 38, wherein the insulating liner is a high absorption material or a thermal oxide material.

40. The processing system of claim 38, wherein the first fill material is selected from the group consisting of doped polysilicon, undoped polysilicon and boron-doped carbon.

41. The processing system of claim 38, wherein the trench has a depth of about 4μm to about 6μm.

42. The processing system of claim 37, further comprising a second fill material that has a higher refractive index than that of the first material.

43. The processing system of claim 38, wherein the integrated circuit comprises one of a CMOS image sensor, a CCD image sensor, a DRAM, a flash memory, an SRAM, a microprocessor, a DSP and an ASIC.

44. An isolation structure provided at a surface of a substrate between a source area in which at least one of photons and charged particles originate and an active region, the isolation structure comprising:

at least one trench extending from the surface of the substrate into the substrate to a depth of at least about 0.5μm and with a length extending across the surface of the substrate between the source area and the active area.

45. An integrated circuit comprising:

a substrate;

an array of pixel cells at a surface of the substrate, each pixel cell comprising a photo-conversion device; and

at least one trench around at least a portion of the array, wherein the trench extends from the surface of the substrate to a depth of at least about 0.5μm into the substrate.

46. A processing system, the processing system comprising:

a processor;

an integrated circuit coupled to the processor, the integrated circuit comprising a structure for isolating an

active area on the integrated circuit, the structure comprising:

a trench extending from a surface of a substrate to a depth of at least about 0.5μm into the substrate.

47. A method of forming a structure for isolating areas in an integrated circuit, the method comprising:

forming a trench having sidewalls in a substrate to separate regions of an integrated circuit, wherein the trench extends below a surface of the substrate to a depth of at least about 0.5μm; and

at least partially filling the trench with a first attenuating material.

48. The method of claim 47, further comprising forming an insulating liner at least along the sidewalls.

49. The method of claim 48, wherein the insulating liner is a high absorption material.

50. The method of claim 48, wherein the insulating liner is a thermal oxide material.

51. The method of claim 47, wherein the substrate is an epitaxial layer.

52. The method of claim 47, wherein the first attenuating material is an attenuating material that absorbs photons.

53. The method of claim 52, wherein the first attenuating material comprises one of doped polysilicon, undoped polysilicon and boron-doped carbon.

54. The method of claim 47, wherein the trench has a depth of about 4μm to about 6μm.

55. The method of claim 47, further comprising the step of partially filling the trench with a second attenuating material, wherein the second material prevents at least a portion of photons from passing through the trench.

56. The method of claim 55, wherein the second attenuating material has a higher refractive index than that of the first attenuating material and is deposited over the surface of the first attenuating material.

57. The method of claim 55, further comprising the step of partially filling the trench with a third attenuating material, wherein the third material prevents at least a portion of photons from passing through the trench.

58. The method of claim 57, wherein the third attenuating material has a higher refractive index than that of the second attenuating material and is deposited over the surface of the second attenuating material.

59. A method of forming a trench structure for isolating areas in an integrated circuit, the method comprising:

forming at least one trench having sidewalls in a substrate to separate regions of an integrated circuit, wherein the trench extends below a surface of the substrate and to a depth of at least about 0.5μm into the substrate.

60. The method of claim 59, further comprising at least partially filling the trench with a first attenuating material.

61. The method of claim 60, further comprising forming an insulating liner at least along the sidewalls of the trench.

62. The method of claim 61, wherein the insulating liner is a high absorption material.

63. The method of claim 61, wherein the insulating liner is a thermal oxide material.

64. The method of claim 60, wherein the first attenuating material comprises one of doped polysilicon, undoped polysilicon and boron-doped carbon.

65. The method of claim 60, further comprising the step of partially filling the trench with a second attenuating material, wherein the second material prevents at least a portion of photons from passing through the trench.

66. The method of claim 65, wherein the second attenuating material has a higher refractive index than that of the first attenuating material and is deposited over the surface of the first attenuating material.

67. The method of claim 65, further comprising the step of partially filling the trench with a third attenuating material, wherein the third material prevents at least a portion of photons from passing through the trench.

68. The method of claim 67, wherein the third attenuating material has a higher refractive index than that of the second attenuating material and is deposited over the surface of the second attenuating material.